Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1. A computer system, the computer system comprising:
a processor for controlling operations of the computer system;
a dynamic random access memory (DRAM) electrically connected to the processor for storing data;
a south bridge chipset electrically connected to the processor and the DRAM, the south bridge chipset comprising:
a system controller for controlling operations of the south bridge chipset;
a buffer for temporarily storing the data;
a memory controller for accessing the data in the DRAM;
an integrated device electronics controller (IDE controller) for accessing data in an integrated device electronics (IDE) component; and
a data conversion circuit electrically connected to the memory controller and the IDE controller for converting a hard-disk access command transmitted from the system controller to the IDE controller into a memory access command of the memory controller wherein the memory controller accesses the buffer and the DRAM by execut-

ing the memory access command;
a power supply for generating a plurality of operating voltages to drive the computer system; and
a battery device for generating the operating voltages that self-refresh the DRAM;
wherein when the computer system performs a power supply management operation consistent with an advanced mode and an advanced configuration and power interface (ACPI) and enters a power-saving mode, the computer system can make use of the battery device to constantly self-refresh the DRAM for maintaining the data stored in the DRAM.

[c2] 2. The computer system of claim 1 further comprising a switch electrically connected to the battery device wherein when the computer system enters the power-saving mode, the power supply ceases providing the operating voltage for self-refreshing the DRAM, and the switch will be enabled to make the battery device provide the operating voltage for self-refreshing the DRAM, wherein the power-saving mode comprises a S4 status and a S5 status.

[c3] 3. The computer system of claim 1, wherein the battery device is a rechargeable battery.

[c4] 4. The computer system of claim 1, wherein when the

computer system is powered-on, the power supply will provide the operating voltage for refreshing the DRAM and the switch will be disabled, and then the power supply will charge the battery device.

[c5] 5. The computer system of claim 1, wherein the memory controller accesses an input data temporally stored in the buffer of the south bridge chipset according to the memory access command, and the input data will be stored in the DRAM.

[c6] 6. The computer system of claim 1, wherein the memory controller accesses an output data in the DRAM according to the memory access command, and the output data will be stored in the buffer of the south bridge chipset.

[c7] 7. The computer system of claim 1 further comprising a basic input/output system (BIOS) for executing a power on self test (POST) of the computer system, wherein the BIOS executes the POST and divides the DRAM into a first memory section and a second memory section, and the second memory section is set as a memory capacity that can be used for the operating system of the computer system and the first memory section can be accessed by the memory access command corresponding to the hard-disk access command.

[c8] 8. The computer system of claim 7, wherein the DRAM comprises at least two memory modules installed in two memory slots of the computer system respectively, and one of the memory modules corresponds to a first memory section and the other memory module corresponds to a second memory section.

[c9] 9. The computer system of claim 8, wherein the DRAM comprises a memory module installed in a memory slot of the computer system.

[c10] 10. A method for storing data in a computer system, the computer system comprising a processor for controlling operations of the computer system, a dynamic random access memory (DRAM) electrically connected to the processor for storing the data, a south bridge chipset electrically connected to the processor and the DRAM for converting a hard-disk access command into a memory access command and for executing the memory access command corresponding to the hard-disk access command to access the DRAM, a power supply for generating a plurality of operating voltages to drive the computer system, and a battery device for providing the operating voltage that self-refreshes the DRAM, the method comprising:

providing the battery device to constantly self-refresh the DRAM for maintaining the data stored in the DRAM

when the computer system performs a power supply management operation consistent with an advanced mode and an advanced configuration and power interface (ACPI) and enters a power-saving mode.

[c11] 11. The method of claim 10, wherein the battery device is a rechargeable battery.

[c12] 12. The method of claim 11, wherein when the computer system is powered-on, the power supply will provide the operating voltage for refreshing the DRAM and a switch will be disabled, and then the power supply will charge the battery device.

[c13] 13. The method of claim 10, wherein the power-saving mode comprises a S4 status.

[c14] 14. The method of claim 10, wherein the power-saving mode comprises a S5 status.

[c15] 15. The method of claim 10, wherein the memory controller accesses an output data in the DRAM according to the memory access command, and the output data will be stored in the buffer of the south bridge chipset.

[c16] 16. The method of claim 10, wherein the computer system further comprises a basic input/output system (BIOS) for executing a power on self test (POST) of the

computer system, the method further comprising:
executing the POST and dividing the DRAM into a first memory section and a second memory section; and
setting the second memory section as a memory capacity that can be used for the operating system of the computer system;
wherein the first memory section can be accessed by the memory access command corresponding to the hard-disk access command.

[c17] 17. The method of claim 16, wherein the DRAM comprises at least two memory modules respectively installed in two memory slots of the computer system, and one of the memory modules corresponds to the first memory section and the other memory module corresponds to the second memory section.

[c18] 18. The method of claim 16, wherein the DRAM comprises a memory module installed in a memory slot of the computer system.

[c19] 19. A method for storing data in a computer system, the computer system comprising a processor for controlling operations of the computer system, a dynamic random access memory (DRAM) electrically connected to the processor for storing the data, a south bridge chipset electrically connected to the processor and the DRAM for

converting a hard-disk access command into a memory access command and for executing the memory access command corresponding to the hard-disk access command to access the DRAM, the method comprising:
a data maintaining method for providing a battery device to constantly self-refresh the DRAM for maintaining the data stored in the DRAM when the computer system performs a power supply management operation consistent with an advanced mode and an advanced configuration and power interface (ACPI) and enters a power-saving mode.

[c20] 20. The method of claim 19, wherein the computer system further comprises the battery device electrically connected to the south bridge chipset for providing the operating voltage that self-refreshes the DRAM

21. The method of claim 19, wherein the computer system further comprises a switch electrically connected to the battery device wherein when the computer system enters the power-saving mode, the power supply ceases providing the operating voltage for self-refreshing the DRAM, and the switch will be enabled to make the battery device provide the operating voltage for self-refreshing the DRAM.

[c21] 22. The method of claim 21, wherein the power-saving mode comprises a S4 status.

[c22] 23. The method of claim 21, wherein the power-saving mode comprises a S5 status.